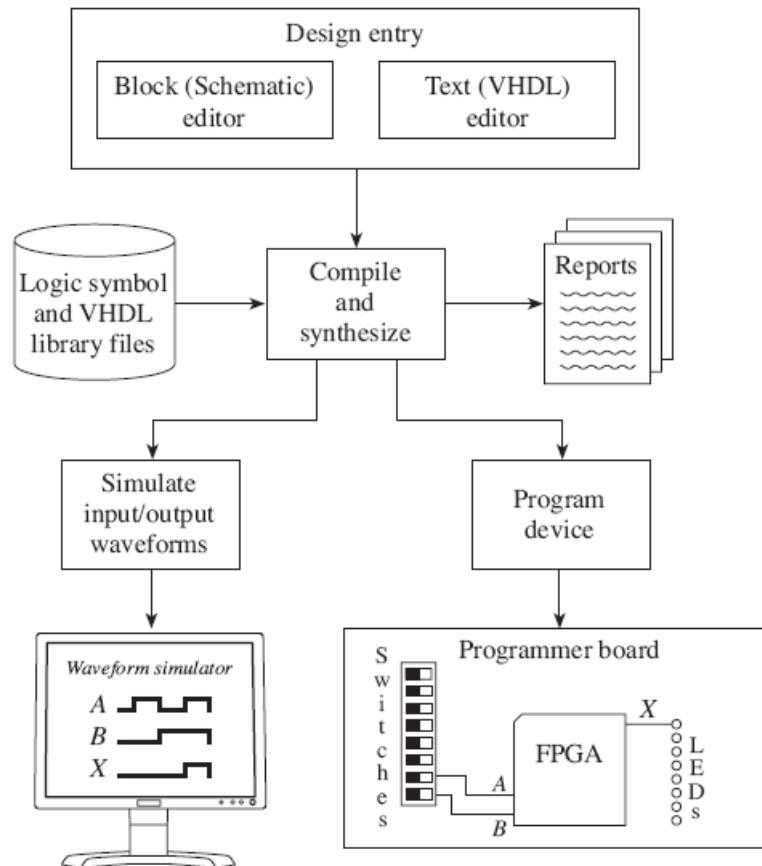
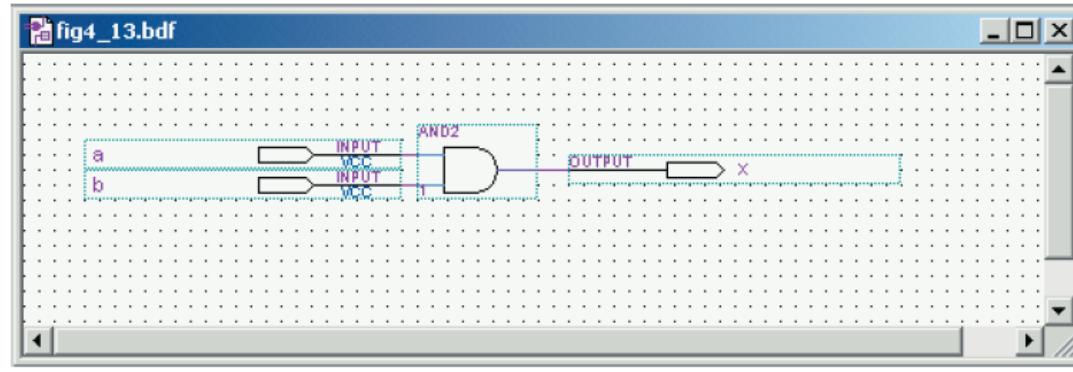


FPGA i VHDL

Od dizajna do realizacije



VHDL primer



(a)

The VHDL code defines an entity named 'Fig4_13' with two inputs ('a' and 'b') and one output ('x'). It also defines an architecture named 'arc' for this entity, which contains a simple logic expression: 'x <= a AND b;'. The code is annotated with callouts:

- Library Declaration:** LIBRARY ieee; USE ieee.std_logic_1164.all; → Declare which VHDL library to use
- Entity declaration:** ENTITY Fig4_13 IS
PORT(
a, b: IN std_logic;
x: OUT std_logic);
END Fig4_13; → Entity name
- Architecture body:** ARCHITECTURE arc OF Fig4_13 IS
BEGIN
x <= a AND b;
END arc; → Define the logic
→ Architecture name

Line 17 Col 1 INS ↻

Altera Quartus Tutorial

- Pročitati:
 - Digital Electronics – A practical Approach With VHDL 9th edition pp. 126-155.

Kombinaciona kola i minimizacija

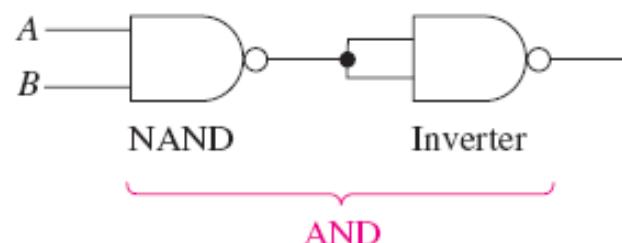
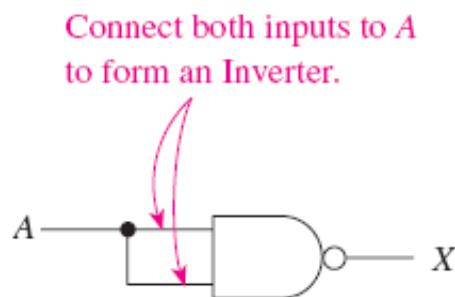
- Pročitati:
 - Digital Electronics – A practical Approach With VHDL 9th edition, Poglavlje 5, sa fokusom na 5-6, 5-7, 5-8 i 5-9.

Primer

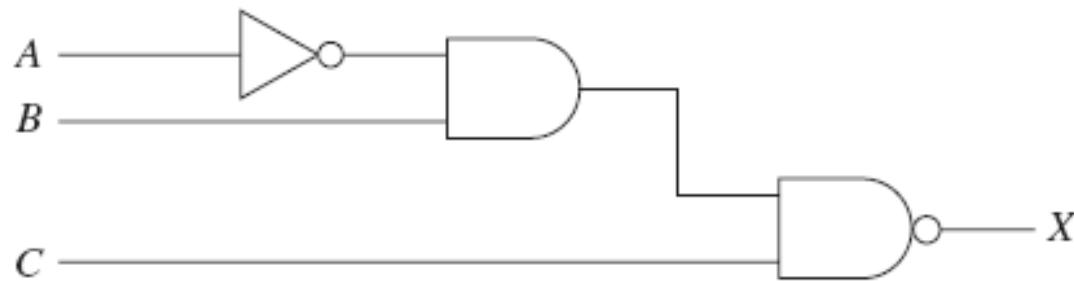
- Modelovati ovu tabelu korišćenjem VHDL-a:

Inputs			Output
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Univerzalna logička kola NAND i NOR

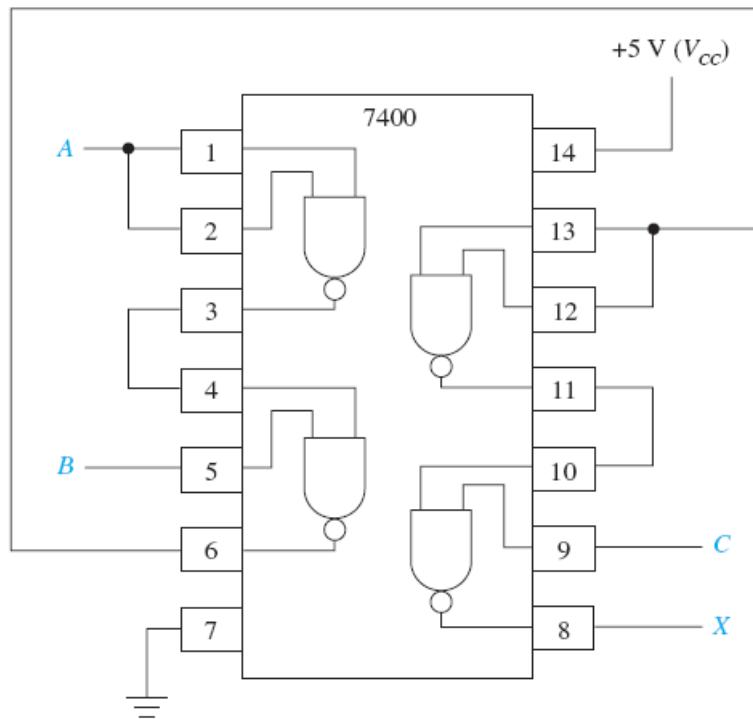


Kako OR?
Kako NOR?



Kako ovo napraviti samo pomoću NAND-ova?

7400 TTL IC



Domaći

- Za domaći sve ovo preko NOR-ova?
 - Inverter
 - OR
 - AND
 - NAND
- Napraviti blok dijagrame i VHDL programe.